Performance Benchmarking of NC-FETs

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Abstract

The negative capacitance field-effect transistor (NC-FET) has emerged as a promising candidate for overcoming the fundamental subthreshold swing (SS) limit in conventional CMOS devices by leveraging ferroelectric-induced voltage amplification. This work analyzes the structure, operation, and performance of NC-FETs across a range of experimentally demonstrated and theoretically projected devices. Benchmarking shows that many devices achieve sub-60 mV/dec switching and improved electrostatic control compared to silicon FinFETs, with HfO_2-based ferroelectrics and gate-all-around (GAA) structures offering the most practical pathways forward. However, challenges such as switching delay, hysteresis, negative differential resistance (NDR), and CMOS integration at advanced nodes remain significant. Ongoing efforts in ferroelectric material engineering, capacitance matching, and device architecture optimization aim to address these limitations. Overall, NC-FETs demonstrate strong potential for next-generation low-power logic, though further advancements are required before widespread technological adoption can be realized.

Introduction

The negative capacitance field-effect transistor (NC-FET) has emerged as a promising device concept aimed at overcoming fundamental limitations in conventional transistor operation. By incorporating a ferroelectric material into the gate stack, NC-FETs exploit the phenomenon of negative capacitance to achieve internal voltage amplification. This allows the gate voltage to more effectively modulate the channel surface potential, enabling subthreshold swings (SS) below the conventional thermal limit of 60 mV/dec at room temperature. As a result, NC-FETs offer the potential to maintain high on-current (I_{ON}) while operating at reduced supply voltages (V_{DD}), making them attractive for low-power and energy-efficient logic applications.

The motivation for NC-FETs arises from the growing challenges faced by traditional CMOS technologies as device dimensions continue to scale. In conventional MOSFETs, the subthreshold swing is fundamentally limited by thermionic carrier transport, which constrains how sharply a device can switch between the OFF and ON states. This limitation prevents further reductions in supply voltage without degrading performance, leading to increased power consumption and reduced efficiency in modern integrated circuits. As scaling progresses into the nanometer regime, these constraints have become a major bottleneck for continued improvements in both performance and energy efficiency.

NC-FETs directly target this limitation by modifying the electrostatics of the gate stack rather than relying solely on geometric scaling. However, despite their strong theoretical advantages, experimental demonstrations of NC-FETs have shown significant variability across device structures, material systems, and fabrication approaches. Implementations range from planar silicon devices and FinFET geometries to transistors based on two-dimensional (2D) materials, often paired with ferroelectric layers such as HfO_2-based films, PZT, or ferroelectric polymers. While some devices report sub-60 mV/dec switching, other key metrics, including on-current, threshold voltage, and operating voltage, vary widely.

Device Structure and Operation

An NC-FET is structurally similar to a conventional MOSFET, except that a ferroelectric layer is incorporated into the gate stack together with the dielectric. In a standard MOSFET, the gate voltage controls

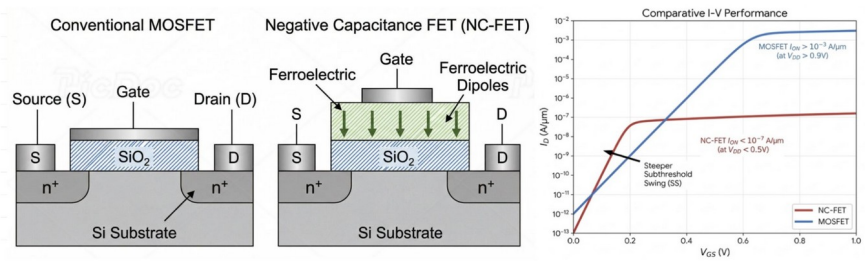


Fig. 1. Comparison of a conventional MOSFET and an NCFET cross section and I-V performace. The NCFET adds a ferroelectric layer to the gate stack so that the gate can control the channel surface potential more efficiently. Adapted from Aaron Frankin et al. Duke ECE 512 Lec 20, Slide 13

conduction between source and drain by modulating the channel potential through a positive gate dielectric. In an NC-FET, the ferroelectric is added to improve this gate control, with the goal of achieving steeper switching and lower-voltage operation than in a conventional transistor. This basic structure is illustrated in Fig. 1.

In any field-effect transistor, the switching sharpness is described by the subthreshold swing:

$$SS = \frac{dV_G}{d(\log_{10} I_D)} = \frac{dV_G}{d\psi_s} \cdot \frac{d\psi_s}{d(\log_{10} I_D)}$$

where the first term describes how efficiently the gate voltage modulates the channel potential, and the second term describes how the channel potential changes the drain current.

In a conventional MOSFET, the first term is limited by the gate-stack capacitance $\frac{dV_G}{d\psi_s} = 1 + \frac{C_s}{C_{ins}}$ where C_s is the semiconductor capacitance and C_{ins} is the insulator capacitance. Because both capacitances are positive in a conventional MOSFET, this term is always greater than 1, which leads to the well-known thermal limit of about 60 mV/dec at room temperature. In other words, some portion of the applied gate voltage is lost across the gate stack before it can modulate the channel.

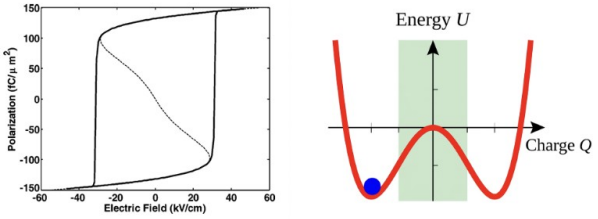


Fig. 2. Illustration of negative-capacitance gate-stack behavior in an NC-FET. Redeveloped from S. Salahuddin

Unlike an ordinary dielectric, a ferroelectric has an energy landscape with two stable polarization states, often represented as a double-well potential, as illustrated in Fig. 2. Around the unstable region between these two minima, the curvature of the energy profile is negative, which corresponds to a negative differential capacitance regime. Physically, this means that as charge increases, the incremental voltage across the ferroelectric can decrease rather than increase. When the ferroelectric is placed in series with a conventional dielectric, this negative-capacitance behavior can offset part of the voltage that would otherwise be lost across the gate stack. The result is that the internal channel potential can respond more strongly than in a conventional MOSFET. Equivalently, the ferroelectric acts like a voltage transformer inside the gate stack, boosting the effectiveness of the applied gate bias and, in principle, enabling sub-60 mV/dec switching.

A ferroelectric layer cannot usually operate in this regime by itself, however, because the negative-capacitance region is not stable in isolation. Practical NC-FETs therefore pair the ferroelectric with a conventional dielectric so that the overall gate stack remains stabilized while still benefiting from internal voltage amplification. In practice, the design must balance this amplification against nonideal effects such as hysteresis and other unstable switching behavior.

McGuire et al. demonstrated this principle experimentally in Fig. 3 [13], showing both steep switching and internal voltage amplification. They reported an HZO-based MoS2 NC-FET in which the ferroelectric gate stack produced a stronger internal channel-control response than in a conventional transistor.

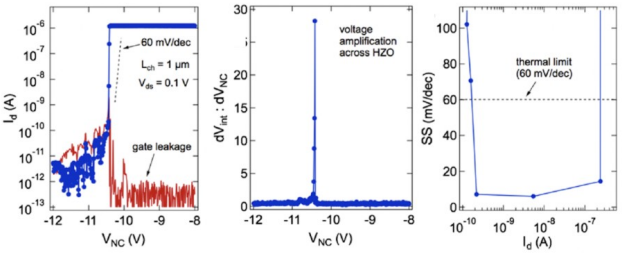


Fig. 3. Representative experimental operation of an HZO-based NCFET from McGuire et al.: (a) transfer characteristics showing steep subthreshold switching (b) internal voltage amplification associated with the ferroelectric gate stack (c) sub-60 subthreshold swing measured.

Although the basic idea remains the same, NC-FETs have been demonstrated in several

device geometries and material systems. Reported structures include planar transistors, FinFET-like or other multi-gate geometries, and 2D-channel devices such as MoS_2 transistors. A range of ferroelectric materials has been explored, including PZT, ferroelectric polymers such as P(VDF-TrFE), and HfO_2-based films. Among these, doped HfO_2-based ferroelectrics are widely regarded as especially promising for practical technology integration because HfO_2 is already used in advanced gate stacks.

Performance Benchmarking

The primary advantage of negative capacitance FETs is the ability to bypass the Boltzmann barrier of thermonic emission and achieve a subthreshold swing below 60 mV/dec. As shown in table 1, the seven experimental and two theoretical NC-FETs all feature subthreshold swings below this barrier. With this decreased subthreshold swing, these devices are all able to obtain faster switching times than industry-standard silicon FETs, which typically feature SS values between 60 and 70 mV/dec.

However, beyond SS it is important to note that because of the recency of NC-FET research spanning a wide range of materials and architectures, it is difficult to directly compare NC-FET experiments solely on the basis of performance metrics. The devices in table 1 vary significantly in structure, operating voltage, and design goals. For example, the printed device reported by Pradhan et al., which focused on demonstrating proof-of-concept farroelectric behaviour and extremely low SS, comes at the sacrifice of extremely high operating voltage (8V), rendering it effectively useless for modern CMOS applications. In contrast, devices like that reported by Tripathi et al., Yan et al., and Seo et al. focus more on low-power logic circuit compatibility, offering marginal threshold voltage improvements over silicon competitors and faster switching speeds by combining nanosheet farroelectrics with finFET architectures.

TABLE 1
DEVICE PERFORMANCE BENCHMARKING

Ref.	Technique	Subthreshold swing (mV/dec)	Remanent polarization ($\mu C/cm^2$)	On-off current ratio (mA/μm)	Threshold voltage (V)
Pradhan et al., ACS Applied Materials & Interfaces, 16 (2024) [4]	Experimental	2.3 (V_{DD} = 8 V)	4.0	1.0 / Not listed	4.3 (V_{ds} = 0.5 V)
Tripathi et al., Scientific Reports, 15, 14081 (2025) [5]	Experimental	30.5 (V_{ds} = 0.3 V)	1.21	1.0 / (1×10^{-9})	0.65
Yan et al., Nanomaterials, 13 (2022) [15]	Experimental	35.4 (Minimum, V_{DD} = 0.1 V)	9.34	4.1×10^7	0.5
Sritharan et al., IEEE Transactions on Nanotechnology, 24, (2025) [6]	Experimental	48.3 (V_{DD} = 0.5 V)	4.0	Not listed	~0.3 (varied by up to 106 mV with different DEs)
Lee et al., IEEE Electron Device Letters, 40, 1708 (2019) [3]	Experimental	26.84 (V_{DD} = 1 V)	21.96% Improvement	10×10^8	0.45
Seo et al., IEEE Transactions on Electron Devices, 64, 1793 (2017) [1]	Experimental	43.5	5.2	12.9 / Not listed	0.25
Mehta et al., IEEE Transactions on Electron Devices, 66, 2904 (2019) [12]	Experimental	44.5 (C_P = 0.8 μF/cm^2)	2.0	11×10^3 (C_P = 0.8 μF/cm^2)	0.114 (C_P = 0.8 μF/cm^2)
Tripathi et al., Scientific Reports, 15, 14081 (2025) [5]	Theoretical	55.54	Not listed	0.01 / (1×10^{-11})	0.43
Valasa et al., ACS Applied Electronic Materials, 6, 3206 (2024) [10]	Theoretical	58.1 (V_{DD} = 0.67 V)	25	3.2×10^{10} Improvement by 54.96%	Not listed
Li et al. ECS J. Solid State Sci. Technol. 13 065007 (2024) [11]	Experimental (Si nanosheet GAA NFET comparison)	68	N/A	2×10^7	0.7

Structurally, nearly all experimental NC-FETs designed for logic applications employ a HfO_2 doped farroelectric into existing gate-all-around or finFET architectures. In every experimental case, these structures offered improved electrostatic gate control while reducing short channel effects, offering the most promising path towards widespread commercialization of NC-FETs in low power electronics.

One of the most critical properties when considering the potential use of negative capacitance FETs in logic applications is remanent polarization (P_r): the residual polarization in a NC-FET after the gate electric field is removed. While a higher P_r can strengthen the negative capacitance effect and improve

voltage amplification, it also increases the likelihood of hysteresis: history dependent polarization in the farroelectric layer. In logic applications, excessive hysteresis is particularly undesirable because it leads to unstable responses in logic circuits and memory-like behavior. This tradeoff is one of the primary points of investigation in the work reported by Mehta et al., which investigates the role of parasitic capacitance in stabilizing NC-FET behavior. The results show that by increasing parasitic capacitance, the remanent polarization can be reduced while simultaneously improving on/off current ratio, improving low power performance. This relationship further complicates benchmarking between NC-FETs, as device performance is not solely dependent on farroelectric strength but also on careful capacitance matching in the gate stack.

The reported on/off ratios further demonstrate this point. While several devices in table 1 exhibit steep subthreshold slopes, their reported current ratios are largely incomplete, making this a target of theoretical experiments like those reported by Tripathi et al. and Valasa et al. These simulations explore employing ultra-thin farroelectric layers and dielectric manipulation to achieve both sub-60 mV/dec subthreshold swings and significantly reduced leakage currents. These findings suggest that, with proper parasitic capacitance, NC-FETs could outperform traditional devices in both switching speed and power consumption. Presently however, despite being unable to improve upon 60 mV/dec SS, silicon GAA and finFET's superior drive current, stability, and manufacturability makes them a far more reliable option for commercial applications than NC-FETs.

Challenges

Despite their strong theoretical advantages, NC-FETs face several key challenges that limit practical implementation. One major issue is switching delay, arising from the finite polarization dynamics of the ferroelectric (FE) layer. Domain switching introduces latency, creating a tradeoff between steep subthreshold swing (SS) and high-speed operation. Addressing this is difficult because polarization switching is an intrinsic material property, but current approaches focus on thinner FE layers, faster-switching materials (e.g., optimized HfO_2-based films), and improved interface engineering.

A second challenge is hysteresis and stability. The negative capacitance effect originates from an unstable region of the ferroelectric polarization curve, requiring precise capacitance matching with the dielectric. Poor matching leads to hysteresis and non-ideal switching, which is unacceptable for logic applications. This is difficult due to variability in material properties and fabrication, but researchers are working on dielectric–FE co-design, thickness optimization, and phase engineering of HfO_2 to stabilize operation and minimize hysteresis.

Negative Differential Resistance (NDR) can also occur when the FE layer is too thick or improperly matched, pushing the device into an unstable regime. This degrades output characteristics and can cause circuit-level instability. Efforts to mitigate NDR focus on careful capacitance balancing, scaling down FE thickness, and using advanced device architectures (e.g., GAA/nanosheet structures) to improve electrostatic control.

Finally, manufacturing and scalability remain major barriers. Integrating ferroelectric materials into standard CMOS flows while maintaining uniformity and reliability at advanced nodes (2.5–5 nm) is highly challenging due to tight process tolerances and material variability. Although HfO_2-based ferroelectrics are promising for CMOS compatibility, achieving consistent large-scale fabrication is difficult. Current solutions include leveraging existing high-κ processes, improving deposition and annealing techniques, and developing process flows compatible with advanced node architectures.

Conclusion

Compared to industry-standard transistors, NCFETs clearly demonstrate superior subthreshold behavior, but do not yet compete as logic devices because of the required nuances of balancing parasitic capacitance to avoid hysteresis and variability in material properties. As the research progresses, there remains a potential for improvements to allow for advances in manufacturing and hysteresis behavior across device dimensions, eventually offering the possibility to integrate NCFETs in low-power or high speed computing applications, although currently they remain a purely experimental device.

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